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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,874	11/26/2003	Takashi Kobayashi	XA-10000	6095

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EXAMINER	
DICKEY, THOMAS L	
ART UNIT	**PAPER NUMBER**
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/721,874	KOBAYASHI ET AL.	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *28 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-21,23-29 and 42-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-21,23-29 and 42-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 2/28/07 has been entered.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Response to Arguments

3. Applicant's arguments filed 2/28/07 have been fully considered.

It is argued, at page 27 of the remarks, that "Applicants initially observe that the primary reference to Eitan fails to teach a silicon 'nitride dots charge trapping layer 54' as asserted in the rejection. Rather, as was pointed out in the Response dated June 12, 2006, Eitan discloses that layer 54 is a silicon dioxide layer with buried polysilicon islands 57." The Examiner notes, however, that Applicants have cited (without a translation, even partial, or any explanation of relevance) JP-05-75133. In commonly assigned Application No. 10/600,344, now Patent No. 6,867,455, Applicants' colleagues Itoh et al. state, " A technique for forming a silicon nitride film like a dot in a silicon oxide film in place of the silicon dot has been described in [JP-05-75133] (see FIG. 1 in the publication), for example. In a dot-like silicon nitride film, the movement of the held electric charge is caused with more difficulty than that in the continuous film of the gate insulat-

ing film 120. Thus, it is possible to suppose that the same effects as those of the silicon dot DT can be obtained." Note paragraph 0155 of Itoh et al. Itoh and colleagues (and presumably Applicants as well) thus clearly understood that Eitan's buried polysilicon islands 57 could be freely interchanged with the claimed "silicon nitride dots," using techniques taught as early as 1993, in JP-05-75133.

This examiner further notes that Itoh et al. make clear in their specification and arguments that their invention is an improvement-style invention of the sort Judge Rich characterized, in *Kimberly-Clark Corporation v. Johnson & Johnson and Personal Products Company*, 223 USPQ 603 (Fed. Cir. 1984), as an "invention which we find nonobvious ... specifically claimed in the patent in suit, a narrow invention in a crowded art." On the other hand Applicants' specification, and especially Applicants' arguments, create the impression that Applicants have pioneered the use of each every element of Applicants' rather lengthy claims, from the "first and second semiconductor regions formed in a semiconductor substrate," to the "silicon nitride dots sandwiched between first and second insulator films, said films being larger in barrier height than silicon nitride," to the "programming performed by injecting charges from said channel region into said silicon nitride dots on a first end portion of said channel region on a side of said first semiconductor region or into said silicon nitride dots on a second end portion of said channel region on a side of said second semiconductor region."

Applicants have every right to insist that the Examiner provide strict proof showing each and every element found in the claims to be anticipated (either explicitly or inher-

ently) or obvious, no matter how familiar a given element may appear. But it can be a lengthy process. Note that commonly assigned Application No. 10/600,344, which provides a clear indication of the context of its claims, issued more than two years ago, although it was filed only five months before the instant application. Applicants' amended claims, on the other hand, show no sign of being allowable.

It is argued, at page 28 of the remarks, that "Applicants would additionally observe with respect to Taira, however, that the rejection seems to confuse the concept of layer thickness or physical height and that of 'barrier height' as recited in the claims. The concepts are quite distinct, as is well understood in the art."

The use of silicon oxide (which has a band-gap of about 11 electron-volts) to "trap" both electrons and holes in a silicon nitride (band-gap of 8 electron-volts) dot is in fact well known in the art. See, e.g. figures 5 and 6 and column 4 lines 4-25 of Papadas 6,218,700. Note especially figure 6, where Papadas shows that thermal electrons and holes at the respective bottoms and tops of the respective conduction and valence bands of Si_3N_4 layers 14 and 15 are surrounded by SiO_2 layers 11,12, and 13 which, by virtue of the larger band-gap of SiO_2, offer no available quantum states through which said thermal electrons and holes can move, in the adjacent SiO_2 layers. Since these electrons/holes cannot move through the adjacent layers, they are "trapped" (as Papadas explains) in the Si_3N_4 layers 14 and 15.

A review of Applicants' specification, however, offers nary a clue that Applicants intend their "barriers" to operate using this well-known principle. Were the Examiner to

attempt to "read" Applicants' claimed barriers onto Papadas' structure including insulators of varying band-gap, Applicants would have the right (see above) to insist on strict proof that this was so. In view of the paucity of information Applicants supply about their own barriers, such proof would be hard to come by. The only thing one can really know for sure about the claimed barriers is that silicon oxide supplies such a barrier. One knows this for sure because Applicants specifically admit this fact, at paragraph 0133 of the application. It matters not whether silicon oxide provides the "barrier" by virtue of layer thickness, physical height, larger band-gap, chain-link fencing, or what you will. Applicants specifically admit that this particular material supplies the claimed "barrier."

Applicant's argument with respect to the rejection(s) of claim(s) 1,10,20, and 29 under 35 USC 103 is nonetheless persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of, amongst other art, Nakao 5,319,230 (an English language version of JP-05-75133).

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1,20, and 29 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for "first and second insulator films larger in barrier

height than silicon nitride" made from silicon oxide, does not reasonably provide enablement for "first and second insulator films larger in barrier height than silicon nitride" made from, for example, aluminum oxide, calcium fluoride, or hafnium oxide. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims. It appears that Applicants have claimed a genus ("insulator films larger in barrier height [whatever Applicants intend that to mean] than silicon nitride") but taught how to make and use only a single species (silicon oxide).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

A. Claims 1,2,4-7, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by NAKAO (5,319,230).

Nakao discloses a nonvolatile semiconductor memory device a semiconductor substrate 3; (a) a first insulator film 12 formed above said semiconductor substrate 3; (b) silicon nitride dots 21 formed on said first insulator film 12; (c) a second insulator film 15 formed on said silicon nitride dots 21; (d) a first conductive film 16 (Applicant simply

recites "conductive film" in claim 1 but for consistency with claims 10-29 this term has been re-labeled) formed on said second insulator film 15; (e) a first semiconductor region 5 and a second semiconductor region formed in said semiconductor substrate 3; (f) a channel region located between said first semiconductor region 5 and said second semiconductor region, wherein said silicon nitride dots 21 are Si_3N_4 (note that when one puts three silicon atoms together with four nitrogen atoms, one has seven atoms, of which 3/7, (.43) are silicon, and 4/7 (.57) are nitrogen. .57 is 1-.43, and .43 is less than 1, so that Si_3N_4 satisfies the claim 7 condition that the X in Si_xN_{1-x}, when the stoichiometry is "renormalized" so that the total number of atoms is 1.000 (i.e. $0<X<1$), is .43) and (h) said first insulator film 12 and said second insulator film 15 are silicon oxide films and therefore inherently (note paragraph 0133 of the instant application, where Applicants state unequivocally that ""[S]ilicon oxide film is larger in barrier height than silicon nitride") larger in barrier height than silicon nitride, and wherein (note figure 6) said first semiconductor region 5 and said second semiconductor region extend in a first direction, and said first conductive film 16 extends in a second direction orthogonal to said first direction, and said silicon nitride dots 21 are present as a single layer on said first insulator film 12. Note figures 1-4 and column 4 lines 19-50 of Nakao.

The applicant's claims 1,2,4-7, and 9 do not distinguish over the Nakao reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited function of performing programming by injecting charges from said channel region into said silicon nitride dots on a first end portion

of said channel region on a side of said first semiconductor region or into said silicon nitride dots on a second end portion of said channel region on a side of said second semiconductor region, and conducting injection of said charges into said silicon nitride dots on said first end portion by carrying electrons from said second semiconductor region toward said first semiconductor region, injection of said charges into said silicon nitride dots on said second end portion is conducted by carrying electrons from said first semiconductor region toward said second semiconductor region, said charges injected into said silicon nitride dots on said first end portion are determined by carrying the electrons from said first semiconductor region to said second semiconductor region, and said charges injected into said silicon nitride dots on said second end portion are determined by carrying the electrons from said second semiconductor region to said first semiconductor region.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]), makes it clear that it is the patentability of the device per se which must be determined in a "functional language" claim and not the patentability of the function, and that an old or obvious device alleged to perform a new function is not patentable as a device, whether claimed in "functional language" terms or not. Note that caselaw makes clear that in such cases applicant has the burden of showing that a prior art device that

appears reasonably capable of performing the allegedly novel function is in fact incapable of doing so. See *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks") and *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable). See MPEP § 2114.

In *Ex parte* Smith, 83 USPQ2d 1509 (Bd. Pat. App. & Int. 2007, PRECEDENTIAL), the Board found, "There is nothing in the Specification to indicate that the [property] necessary to render the [claimed structure] [capable of the clamed function] is anything more than the inherent result of constructing the [claimed structure] of standard materials in accordance with claim 35's other limitations, which are expressly disclosed in [the prior art]." The Board held, "We thus agree with the Examiner that a prima facie case of anticipation is established by [the prior art]. Because the Appellant presented no evidence to overcome the Examiner's finding of the inherent ability of [the prior art's] [structure] to [perform the clamed function], she failed to meet her burden to overcome that prima facie case. We therefore find that claim 35 is anticipated by [the prior art]." The Board cited *In re King* for the proposition that "[A] prima facie case of anticipation [may be] based on inherency," and *In re Best* for the proposition that "Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by

identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product," in support if its holding. See *Ex parte* Smith, 83 USPQ2d 1509,1514 (Bd. Pat. App. & Int. 2007).

In this case it is reasonable to assume that Nakao's device is capable of performing programming by injecting charges from said channel region into said silicon nitride dots on a first end portion of said channel region on a side of said first semiconductor region or into said silicon nitride dots on a second end portion of said channel region on a side of said second semiconductor region, and conducting injection of said charges into said silicon nitride dots on said first end portion by carrying electrons from said second semiconductor region toward said first semiconductor region, injection of said charges into said silicon nitride dots on said second end portion is conducted by carrying electrons from said first semiconductor region toward said second semiconductor region, said charges injected into said silicon nitride dots on said first end portion are determined by carrying the electrons from said first semiconductor region to said second semiconductor region, and said charges injected into said silicon nitride dots on said second end portion are determined by carrying the electrons from said second semiconductor region to said first semiconductor region, because a comparison of Applicant's specification to Nakao's disclosure reveals that Nakao discloses a device that is apparently identical to the device Applicant describes as being capable of performing the function of performing programming by injecting charges from said channel region into said silicon nitride

dots on a first end portion of said channel region on a side of said first semiconductor region or into said silicon nitride dots on a second end portion of said channel region on a side of said second semiconductor region, and conducting injection of said charges into said silicon nitride dots on said first end portion by carrying electrons from said second semiconductor region toward said first semiconductor region, injection of said charges into said silicon nitride dots on said second end portion is conducted by carrying electrons from said first semiconductor region toward said second semiconductor region, said charges injected into said silicon nitride dots on said first end portion are determined by carrying the electrons from said first semiconductor region to said second semiconductor region, and said charges injected into said silicon nitride dots on said second end portion are determined by carrying the electrons from said second semiconductor region to said first semiconductor region.

Because it is reasonable to assume that assume that Nakao's device is capable of performing the claimed function, the burden shifts to Applicants to show that it are not. See MPEP § 2114.

B. Claims 1,2,4-7,9-16,18,19,29,42,43 and 45 are rejected under 35 U.S.C. 102(b) as being anticipated by OHBA ET AL. (2002/0140023).

With regard to claims 1,2,4-7, and 9 Ohba et al. discloses a nonvolatile semiconductor memory device comprising a semiconductor substrate 11; (a) a first insulator film 14 formed above said semiconductor substrate 11; (b) silicon nitride dots 41 formed on said first insulator film 14; (c) a second insulator film 16 formed on said silicon nitride

dots 41; (d) a first conductive film 17 (Applicant simply recites "conductive film" in claim 1 but for consistency with claims 10-29 this term has been re-labeled) formed on said second insulator film 16; (e) a first semiconductor region 18 and a second semiconductor region 19 formed in said semiconductor substrate 11; (f) a channel region 20 located between said first semiconductor region 18 and said second semiconductor region 19, wherein said silicon nitride dots 41 are Si_3N_4 (note that when one puts three silicon atoms together with four nitrogen atoms, one has seven atoms, of which 3/7, (.43) are silicon, and 4/7 (.57) are nitrogen..57 is 1-.43, and.43 is less than 1, so that Si_3N_4 satisfies the claim 7 condition that the X in Si_xN_{1-x}, when the stoichiometry is "renormalized" so that the total number of atoms is 1.000 (i.e. $0<X<1$), is.43) and (h) said first insulator film 14 and said second insulator film 16 are SiO_2 (Si_xO_2, where $x<=1$) silicon oxide films and therefore inherently (note paragraph 0133 of the instant application, where Applicants state unequivocally that ""[S]ilicon oxide film is larger in barrier height than silicon nitride") larger in barrier height than silicon nitride, and said first semiconductor region 18 and said second semiconductor region 19 extend in a first direction, said silicon nitride dots 41 are present as a single layer on said first insulator film 14, and said first conductive film 17 extends in a second direction orthogonal to said first direction. Note figure 8 and paragraphs 0154-0163 of Ohba et al.

The applicant's claims 1,2,4-7, and 9 do not distinguish over the Ohba et al. reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited function of performing programming by

injecting charges from said channel region into said silicon nitride dots on a first end portion of said channel region on a side of said first semiconductor region 18 or into said silicon nitride dots on a second end portion of said channel region on a side of said second semiconductor region, and conducting injection of said charges into said silicon nitride dots on said first end portion by carrying electrons from said second semiconductor region toward said first semiconductor region, injection of said charges into said silicon nitride dots on said second end portion is conducted by carrying electrons from said first semiconductor region toward said second semiconductor region, said charges injected into said silicon nitride dots on said first end portion are determined by carrying the electrons from said first semiconductor region to said second semiconductor region, and said charges injected into said silicon nitride dots on said second end portion are determined by carrying the electrons from said second semiconductor region to said first semiconductor region.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]), makes it clear that it is the patentability of the device per se which must be determined in a "functional language" claim and not the patentability of the function, and that an old or obvious device alleged to perform a new function is not patentable as a device, whether claimed in "functional language" terms or not. Note that caselaw makes

clear that in such cases applicant has the burden of showing that a prior art device that appears reasonably capable of performing the allegedly novel function is in fact incapable of doing so. See *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks") and *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable). See MPEP § 2114.

In *Ex parte* Smith, 83 USPQ2d 1509 (Bd. Pat. App. & Int. 2007, PRECEDENTIAL), the Board found, "There is nothing in the Specification to indicate that the [property] necessary to render the [claimed structure] [capable of the clamed function] is anything more than the inherent result of constructing the [claimed structure] of standard materials in accordance with claim 35's other limitations, which are expressly disclosed in [the prior art]." The Board held, "We thus agree with the Examiner that a prima facie case of anticipation is established by [the prior art]. Because the Appellant presented no evidence to overcome the Examiner's finding of the inherent ability of [the prior art's] [structure] to [perform the clamed function], she failed to meet her burden to overcome that prima facie case. We therefore find that claim 35 is anticipated by [the prior art]." The Board cited *In re King* for the proposition that "[A] prima facie case of anticipation [may be] based on inherency," and *In re Best* for the proposition that "Where, as here, the

claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product," in support if its holding. See *Ex parte* Smith, 83 USPQ2d 1509,1514 (Bd. Pat. App. & Int. 2007).

In this case it is reasonable to assume that Ohba et al.'s device is capable of performing programming by injecting charges from said channel region into said silicon nitride dots on a first end portion of said channel region on a side of said first semiconductor region or into said silicon nitride dots on a second end portion of said channel region on a side of said second semiconductor region, and conducting injection of said charges into said silicon nitride dots on said first end portion by carrying electrons from said second semiconductor region toward said first semiconductor region, injection of said charges into said silicon nitride dots on said second end portion is conducted by carrying electrons from said first semiconductor region toward said second semiconductor region, said charges injected into said silicon nitride dots on said first end portion are determined by carrying the electrons from said first semiconductor region to said second semiconductor region, and said charges injected into said silicon nitride dots on said second end portion are determined by carrying the electrons from said second semiconductor region to said first semiconductor region, because a comparison of Applicant's specification to Ohba et al.'s disclosure reveals that Ohba et al. discloses a device that is apparently identical to the device Applicant describes as being capable of

performing the function of performing programming by injecting charges from said channel region into said silicon nitride dots on a first end portion of said channel region on a side of said first semiconductor region or into said silicon nitride dots on a second end portion of said channel region on a side of said second semiconductor region, and conducting injection of said charges into said silicon nitride dots on said first end portion by carrying electrons from said second semiconductor region toward said first semiconductor region, injection of said charges into said silicon nitride dots on said second end portion is conducted by carrying electrons from said first semiconductor region toward said second semiconductor region, said charges injected into said silicon nitride dots on said first end portion are determined by carrying the electrons from said first semiconductor region to said second semiconductor region, and said charges injected into said silicon nitride dots on said second end portion are determined by carrying the electrons from said second semiconductor region to said first semiconductor region.

Because it is reasonable to assume that assume that Ohba et al.'s device is capable of performing the claimed function, the burden shifts to Applicants to show that it are not. See MPEP § 2114.

With regard to claims 10-16,18, and 19 Ohba et al. discloses a nonvolatile semiconductor memory device comprising a semiconductor substrate 11; a first semiconductor region 18 and a second semiconductor region 19 formed in said semiconductor substrate 11; (b) a channel region 20 located between said first semiconductor region 18 and said second semiconductor region 19; (c) a first insulator film 14 formed above said

semiconductor substrate 11, and extending from above said channel region 20 toward above said first semiconductor region 18; (d) silicon nitride dots 41 formed on said first insulator film 14; (e) a second insulator film 16 formed on said silicon nitride dots 41; and (f) a first conductive film 17 formed on said second insulator film 16; wherein said silicon nitride dots 41 are Si_3N_4 (note that when one puts three silicon atoms together with four nitrogen atoms, one has seven atoms, of which 3/7, (.43) are silicon, and 4/7 (.57) are nitrogen..57 is 1-.43, and.43 is less than 1, so that Si_3N_4 satisfies the claim 16 condition that the X in Si_xN_{1-x}, when the stoichiometry is "renormalized" so that the total number of atoms is 1.000 (i.e. 0<X<1), is.43) and (j) said first insulator film 14 is a thermal SiO_2 film, and said second insulator film 16 is a deposited SiO_2 film so that said first insulator film 14 and said second insulator film 16 are SiO_2 (Si_xO_2, where x<=1) silicon oxide films and therefore inherently (note paragraph 0133 of the instant application, where Applicants state unequivocally that ""[S]ilicon oxide film is larger in barrier height than silicon nitride") larger in barrier height than silicon nitride; further comprising (g) a third insulator film 12 (claim 10 recites just plain "insulator film" but for consistency with claims 20-29 the Examiner has re-labeled it) formed above said semiconductor substrate 11, and extending from above said channel region 20 toward above said second semiconductor region 19; and (h) a second conductive film 13 formed on said third insulator film 12, wherein said first semiconductor region 18 and said second semiconductor region 19 extend in a first direction, said first conductive film 17 extends in a second direction orthogonal to said first direction, and said second conductive film 13 extends in

said first direction, said silicon nitride dots 41 are present as a single layer on said first insulator film 14, said first semiconductor region 18 and said second semiconductor region 19 and said first 17 and second 13 conductive films extend in a same direction, and said second conductive film 13 extends to be mounting up above said first conductive film 17. Note figure 8 and paragraphs 0154-0163 of Ohba et al.

The applicant's claims 10-16,18, and 19 do not distinguish over the Ohba et al. reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited function of performing programming by injecting charges from said channel region into said silicon nitride dots on an end portion of said channel region on a side of said second semiconductor region, and conducting injection of said charges into said silicon nitride dots by carrying electrons from said second semiconductor region toward said first semiconductor region, and said charges injected into said silicon nitride dots are determined by carrying the electrons from said first semiconductor region to said second semiconductor region.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]), makes it clear that it is the patentability of the device per se which must be determined in a "functional language" claim and not the patentability of the function, and that an old or obvious device alleged to perform a new function is not patentable as a de-

vice, whether claimed in "functional language" terms or not. Note that caselaw makes clear that in such cases applicant has the burden of showing that a prior art device that appears reasonably capable of performing the allegedly novel function is in fact incapable of doing so. See *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks") and *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable). See MPEP § 2114.

In *Ex parte* Smith, 83 USPQ2d 1509 (Bd. Pat. App. & Int. 2007, PRECEDENTIAL), the Board found, "There is nothing in the Specification to indicate that the [property] necessary to render the [claimed structure] [capable of the clamed function] is anything more than the inherent result of constructing the [claimed structure] of standard materials in accordance with claim 35's other limitations, which are expressly disclosed in [the prior art]." The Board held, "We thus agree with the Examiner that a prima facie case of anticipation is established by [the prior art]. Because the Appellant presented no evidence to overcome the Examiner's finding of the inherent ability of [the prior art's] [structure] to [perform the clamed function], she failed to meet her burden to overcome that prima facie case. We therefore find that claim 35 is anticipated by [the prior art]." The Board cited *In re King* for the proposition that "[A] prima facie case of anticipation [may

be] based on inherency," and *In re Best* for the proposition that "Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product," in support if its holding. See *Ex parte* Smith, 83 USPQ2d 1509,1514 (Bd. Pat. App. & Int. 2007).

In this case it is reasonable to assume that Ohba et al.'s device is capable of performing programming by injecting charges from said channel region into said silicon nitride dots on an end portion of said channel region on a side of said second semiconductor region, and conducting injection of said charges into said silicon nitride dots by carrying electrons from said second semiconductor region toward said first semiconductor region, and said charges injected into said silicon nitride dots are determined by carrying the electrons from said first semiconductor region to said second semiconductor region, because a comparison of Applicant's specification to Ohba et al.'s disclosure reveals that Ohba et al. discloses a device that is apparently identical to the device Applicant describes as being capable of performing the function of performing programming by injecting charges from said channel region into said silicon nitride dots on an end portion of said channel region on a side of said second semiconductor region, and conducting injection of said charges into said silicon nitride dots by carrying electrons from said second semiconductor region toward said first semiconductor region, and said

charges injected into said silicon nitride dots are determined by carrying the electrons from said first semiconductor region to said second semiconductor region.

Because it is reasonable to assume that assume that Ohba et al.'s device is capable of performing the claimed function, the burden shifts to Applicants to show that it are not. See MPEP § 2114.

With regard to claims 29,42,43, and 45 Ohba et al. discloses a nonvolatile semiconductor memory device comprising a semiconductor substrate 11; a first semiconductor region 18 and a second semiconductor region 19 formed in said semiconductor substrate 11; (b) a channel region 20 located between said first semiconductor region 18 and said second semiconductor region 19; (e) a first insulator film 14 (this part is recited in claim 29 as a "second insulator film," but for consistency with claims 1-28 the Examiner has re-numbered it) formed above said semiconductor substrate 11; (f) silicon nitride dots 41 formed on said first insulator film 14; (g) a second insulator film 16 (this part is recited in claim 29 as a "third insulator film," but for consistency with claims 1-28 the Examiner has re-numbered it) formed on said silicon nitride dots 41; and (h) a first conductive film 17 (this part is recited in claim 29 as a "second conductive film," but for consistency with claims 1-28 the Examiner has re-numbered it) formed on said second insulator film 16, wherein said silicon nitride dots 41 are Si_3N_4 (note that when one puts three silicon atoms together with four nitrogen atoms, one has seven atoms, of which 3/7, (.43) are silicon, and 4/7 (.57) are nitrogen..57 is 1-.43, and.43 is less than 1, so that Si_3N_4 satisfies the claim 26 condition that the X in Si_xN_{1-x}, when the stoichiometry is

"renormalized" so that the total number of atoms is 1.000 (i.e. 0<X<1), is.43) and (l) said first insulator film 14 and said second insulator film 16 are silicon oxide films and therefore inherently (note paragraph 0133 of the instant application, where Applicants state unequivocally that ""[S]ilicon oxide film is larger in barrier height than silicon nitride") larger in barrier height than silicon nitride; further comprising (c) a third insulator film 12 (this part is recited in claim 29 as a "first insulator film," but for consistency with claims 1-28 the Examiner has re-numbered it) formed above said semiconductor substrate 11 on said channel region 20; and (d) a second conductive film 13 (this part is recited in claim 29 as a "first conductive film," but for consistency with claims 1-28 the Examiner has re-numbered it) formed on said third insulator film 12, wherein said first insulator film 14 is formed on both sides of said second conductive film 13 and said silicon nitride dots 41 are present as a single layer on said first insulator film 14. Note figure 8 and paragraphs 0154-0163 of Ohba et al.

The applicant's claims 29,42,43, and 45 do not distinguish over the Ohba et al. reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited function of performing programming by injecting charges into said silicon nitride dots adjacent to the both sides of said second conductive film, respectively.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990)

("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]), makes it clear that it is the patentability of the device per se which must be determined in a "functional language" claim and not the patentability of the function, and that an old or obvious device alleged to perform a new function is not patentable as a device, whether claimed in "functional language" terms or not. Note that caselaw makes clear that in such cases applicant has the burden of showing that a prior art device that appears reasonably capable of performing the allegedly novel function is in fact incapable of doing so. See *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks") and *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable). See MPEP § 2114.

In *Ex parte* Smith, 83 USPQ2d 1509 (Bd. Pat. App. & Int. 2007, PRECEDENTIAL), the Board found, "There is nothing in the Specification to indicate that the [property] necessary to render the [claimed structure] [capable of the clamed function] is anything more than the inherent result of constructing the [claimed structure] of standard materials in accordance with claim 35's other limitations, which are expressly disclosed in [the prior art]." The Board held, "We thus agree with the Examiner that a prima facie case of anticipation is established by [the prior art]. Because the Appellant presented no evi-

dence to overcome the Examiner's finding of the inherent ability of [the prior art's] [structure] to [perform the clamed function], she failed to meet her burden to overcome that prima facie case. We therefore find that claim 35 is anticipated by [the prior art]." The Board cited *In re King* for the proposition that "[A] prima facie case of anticipation [may be] based on inherency," and *In re Best* for the proposition that "Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product," in support if its holding. See *Ex parte* Smith, 83 USPQ2d 1509,1514 (Bd. Pat. App. & Int. 2007).

In this case it is reasonable to assume that Ohba et al.'s device is capable of performing programming by injecting charges into said silicon nitride dots adjacent to the both sides of said second conductive film, respectively, because a comparison of Applicant's specification to Ohba et al.'s disclosure reveals that Ohba et al. discloses a device that is apparently identical to the device Applicant describes as being capable of performing the function of performing programming by injecting charges into said silicon nitride dots adjacent to the both sides of said second conductive film, respectively.

Because it is reasonable to assume that assume that Ohba et al.'s device is capable of performing the claimed function, the burden shifts to Applicants to show that it are not. See MPEP § 2114.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 8,17, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over OHBA ET AL. (2002/0140023) in view of Shimizu et al. (5,060,034).

Ohba et al. discloses a nonvolatile semiconductor memory device with all the limitations of claims 8,17, and 44 except the limitation that a surface portion of said silicon nitride dots is higher in nitrogen concentration than a central portion of said silicon nitride dots. Note figure 8 and paragraphs 0154-0163 of Ohba et al.

However, Shimizu et al. discloses a method of making a nonvolatile semiconductor memory device including a step wherein a nitride charge-trapping region is nitrided by a step of plasma nitriding. Shimizu et al. explain, column 7 lines 23-25, that "By the nitriding method, the area 22B of the gate insulating film 22 has a smaller Si/N [i.e., .85 to 1.1. Note that $Si_{.43}N_{.57}$ has an Si/N ratio of .85 to 1.1] composition ratio and loses its hysteresis characteristic." Shimizu et al. thus describe a plasma nitriding step applicable to making oxide-nitride-oxide semiconductor memory devices such as Ohba et al.'s that may predictably succeed in lowering the hysteresis rate of the nitride so formed. Note figure 4A and column 7 lines 17-26 of Shimizu et al. Note that Applicants have ex-

plained, at paragraph 0127 of the application, "Since a plasma nitriding reaction conducted to the silicon dots progresses toward a dot central portion rather than a dot surface, a nitrogen concentration of the dot surface is higher than that of the dot central portion." It would have been obvious to a person having skill in the art to modify Ohba et al.'s nonvolatile semiconductor memory device by making it using the plasma nitriding step taught by Shimizu et al.), thus inherently (according to Applicants) achieving the claimed invention including a surface portion of said silicon nitride dots that is higher in nitrogen concentration than a central portion of said silicon nitride dots.

In a case such as this one, where "an improvement is no more than 'the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for improvement,' *KSR Int'l Co. v. Teleflex Inc.*, [127 S.Ct. 1727, 1740, 82 USPQ2d 1385, 1396 (2007)], no further analysis is required of the Examiner." (emphasis added) *Ex parte* Smith, 83 USPQ2d 1509, 1518 (Bd. Pat. App. & Int. 2007, PRECEDENTIAL).

B. Claims 20,21,23-26, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over CHANG (5,408,115) in view of Ohba et al. (2002/0140023).

Chang discloses a nonvolatile semiconductor memory device comprising a channel region 32 located between a first semiconductor region 16 and a second semiconductor region 18 formed in a semiconductor substrate 10; first and second conductive films 14 formed on first and second insulator films 12 formed above said semiconductor substrate 10 and extending from above said channel region 32 toward said first semicon-

ductor regions 16 and 18 respectively; a third conductive film 30 formed on a silicon nitride film 24 of an ONO layer 20, said ONO layer comprising (note figure 1A) a fourth insulator film 26 formed on the silicon nitride film 24 formed on a third insulator film 22 formed above the semiconductor substrate 10 between said first second conductive films 14; wherein said silicon nitride dots 21 are Si_3N_4 (note that when one puts three silicon atoms together with four nitrogen atoms, one has seven atoms, of which 3/7, (.43) are silicon, and 4/7 (.57) are nitrogen. .57 is 1-.43, and .43 is less than 1, so that Si_3N_4 satisfies the claim 7 condition that the X in Si_xN_{1-x}, when the stoichiometry is "re-normalized" so that the total number of atoms is 1.000 (i.e. $0<X<1$), is .43); and said third insulator film 22 and said fourth insulator film 26 are silicon oxide films and therefore inherently (note paragraph 0133 of the instant application, where Applicants state unequivocally that ""[S]ilicon oxide film is larger in barrier height than silicon nitride") larger in barrier height than silicon nitride. Note figures 1b (showing the details of ONO layer 20 of figure 6) and 6; column 4 lines 18-24 (describing the details of ONO layer 20 in words), and column 8 lines 13-55 of Chang.

The applicant's claims 20,21,23-26, and 28 do not distinguish over the Chang reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited function of performing programming by injecting charges from said channel region into said silicon nitride dots on a first end portion on a side of said first conductive film or into said silicon nitride dots on a second end portion on a side of said second conductive film, and conducting injection of said

charges into said silicon nitride dots on said first end portion by carrying electrons from said first semiconductor region toward said second semiconductor region, injection of said charges into said silicon nitride dots on said second end portion is conducted by carrying electrons from said second semiconductor region toward said first semiconductor region, said charges injected into said silicon nitride dots on said first end portion are determined by carrying the electrons from said second semiconductor region to said first semiconductor region, and said charges injected into said silicon nitride dots on said second end portion are determined by carrying the electrons from said first semiconductor region to said second semiconductor region.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]), makes it clear that it is the patentability of the device per se which must be determined in a "functional language" claim and not the patentability of the function, and that an old or obvious device alleged to perform a new function is not patentable as a device, whether claimed in "functional language" terms or not. Note that caselaw makes clear that in such cases applicant has the burden of showing that a prior art device that appears reasonably capable of performing the allegedly novel function is in fact incapable of doing so. See *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed func-

tion], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks") and *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable). See MPEP § 2114.

In *Ex parte* Smith, 83 USPQ2d 1509 (Bd. Pat. App. & Int. 2007, PRECEDENTIAL), the Board found, "There is nothing in the Specification to indicate that the [property] necessary to render the [claimed structure] [capable of the clamed function] is anything more than the inherent result of constructing the [claimed structure] of standard materials in accordance with claim 35's other limitations, which are expressly disclosed in [the prior art]." The Board held, "We thus agree with the Examiner that a prima facie case of anticipation is established by [the prior art]. Because the Appellant presented no evidence to overcome the Examiner's finding of the inherent ability of [the prior art's] [structure] to [perform the clamed function], she failed to meet her burden to overcome that prima facie case. We therefore find that claim 35 is anticipated by [the prior art]." The Board cited *In re King* for the proposition that "[A] prima facie case of anticipation [may be] based on inherency," and *In re Best* for the proposition that "Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of

his claimed product," in support if its holding. See *Ex parte* Smith, 83 USPQ2d 1509,1514 (Bd. Pat. App. & Int. 2007).

In this case it is reasonable to assume that Chang's device is capable of performing programming by injecting charges from said channel region into said silicon nitride dots on a first end portion on a side of said first conductive film or into said silicon nitride dots on a second end portion on a side of said second conductive film, and conducting injection of said charges into said silicon nitride dots on said first end portion by carrying electrons from said first semiconductor region toward said second semiconductor region, injection of said charges into said silicon nitride dots on said second end portion is conducted by carrying electrons from said second semiconductor region toward said first semiconductor region, said charges injected into said silicon nitride dots on said first end portion are determined by carrying the electrons from said second semiconductor region to said first semiconductor region, and said charges injected into said silicon nitride dots on said second end portion are determined by carrying the electrons from said first semiconductor region to said second semiconductor region, because a comparison of Applicant's specification to Chang's disclosure reveals that Chang discloses a device that is apparently identical to the device Applicant describes as being capable of performing the function of performing programming by injecting charges from said channel region into said silicon nitride dots on a first end portion on a side of said first conductive film or into said silicon nitride dots on a second end portion on a side of said second conductive film, and conducting injection of said charges into said silicon nitride

dots on said first end portion by carrying electrons from said first semiconductor region toward said second semiconductor region, injection of said charges into said silicon nitride dots on said second end portion is conducted by carrying electrons from said second semiconductor region toward said first semiconductor region, said charges injected into said silicon nitride dots on said first end portion are determined by carrying the electrons from said second semiconductor region to said first semiconductor region, and said charges injected into said silicon nitride dots on said second end portion are determined by carrying the electrons from said first semiconductor region to said second semiconductor region. Because it is reasonable to assume that assume that Chang's device is capable of performing the claimed function, the burden shifts to Applicants to show that it is not. See MPEP § 2114.

Chang does not disclose his silicon nitride film 24 made be formed from silicon nitride dots present as a single layer on said third insulator film.

However, Ohba et al. discloses a variety of nonvolatile semiconductor memory devices. One, note embodiment 1 (figure 2) employs a solid layer of germanium 15 as a charge trap. The next, note figure 5(b), employs a solid layer of tungsten, copper, or aluminum as a charge trap. The next, note figure 7(b), employs a silicon nitride layer 45 as a charge trap. The next, note figure 8, employs silicon nitride dots 41 present as a single layer on insulator film 13, as a charge trap. The next four, note figures 9(b), 10(b), 11(b), and 12(b), employ defects 55, 65, 75, or 85 in silicon oxide layer 16 as charge traps. The next two, note figures 13(b) and 14(b), employs germanium or gold dots as a

charge trap. The next, note figure 16(b), again employs silicon nitride dots, this time marked "115" as a charge trap. Figures 15 through 26 continue in like vein, a total of eighteen specific embodiments being disclosed.

Ohba et al.'s disclosure continues describing various materials in various shapes in sizes, all of which (according to Ohba et al.) may be successfully substituted for each other as the charge storing layer of a nonvolatile semiconductor memory device.

Finally, at paragraph 0309, Ohba et al. state, "Further, the charge stored layer 25 [as seen in FIG.27 as a silicon nitride film 25, identical to the silicon nitride film 24 of Chang's ONO layer 20] made of silicon nitride may well be particles [emphasis added] 25 which are made of silicon nitride and which have diameters of 0.5 nm through 20 nm or so, as shown in FIG. 28." This is proof positive that one of skill in the art would have understood that the silicon nitride particles 25 of Ohba et al.'s figure 28 could have been successfully substituted for Chang's silicon film 24, with predictable results. It would therefor have been obvious to a person having skill in the art to modify Chang's non-volatile semiconductor memory device by substituting Ohba et al.'s silicon nitride dots present as a single layer on said third insulator film for Chang's silicon nitride film 24, thus achieving the claimed invention.

Note that Ohba et al.'s disclosure contains ample evidence that one of skill in the art could have made the substitution required to achieve the claimed device, and the result would have been predictable to that person of skill in the art. In a case such as this one, where "an improvement is no more than 'the simple substitution of one known element

for another or the mere application of a known technique to a piece of prior art ready for improvement,' *KSR Int'l Co. v. Teleflex Inc.*, [127 S.Ct. 1727, 1740, 82 USPQ2d 1385, 1396 (2007)], no further analysis is required of the Examiner." (emphasis added) *Ex parte* Smith, 83 USPQ2d 1509, 1518 (Bd. Pat. App. & Int. 2007, PRECEDENTIAL).

C. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over CHANG (5,408,115) in view of Ohba et al. (2002/0140023), as applied to claim 20, above, and further in view of Shimizu et al. (5,060,034).

Chang discloses a nonvolatile semiconductor memory device with all the limitations of claim 27 except the limitation that a surface portion of said silicon nitride dots is higher in nitrogen concentration than a central portion of said silicon nitride dots. Note figures 1b (showing the details of ONO layer 20 of figure 6) and 6; column 4 lines 18-24 (describing the details of ONO layer 20 in words), and column 8 lines 13-55 of Chang, and figures 27-28 and paragraph 0307 of Ohba et al.

However, Shimizu et al. discloses a method of making a nonvolatile semiconductor memory device including a step wherein a nitride charge-trapping region is nitrided by a step of plasma nitriding. Shimizu et al. explain, column 7 lines 23-25, that "By the nitriding method, the area 22B of the gate insulating film 22 has a smaller Si/N [i.e., .85 to 1.1. Note that $Si_{.43}N_{.57}$ has an Si/N ratio of .85 to 1.1] composition ratio and loses its hysteresis characteristic." Shimizu et al. thus describe a plasma nitriding step applicable to making oxide-nitride-oxide semiconductor memory devices such as Chang's that may predictably succeed in lowering the hysteresis rate of the nitride so formed. Note figure

4A and column 7 lines 17-26 of Shimizu et al. Note that Applicants have explained, at paragraph 0127 of the application, "Since a plasma nitriding reaction conducted to the silicon dots progresses toward a dot central portion rather than a dot surface, a nitrogen concentration of the dot surface is higher than that of the dot central portion." It would have been obvious to a person having skill in the art to modify Chang's nonvolatile semiconductor memory device by making it using the plasma nitriding step taught by Shimizu et al.), thus inherently (according to Applicants) achieving the claimed invention including a surface portion of said silicon nitride dots that is higher in nitrogen concentration than a central portion of said silicon nitride dots.

In a case such as this one, where "an improvement is no more than 'the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for improvement,' *KSR Int'l Co. v. Teleflex Inc.*, [127 S.Ct. 1727, 1740, 82 USPQ2d 1385, 1396 (2007)], no further analysis is required of the Examiner." (emphasis added) *Ex parte* Smith, 83 USPQ2d 1509, 1518 (Bd. Pat. App. & Int. 2007, PRECEDENTIAL).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Sue A. Purvis, at 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thomas L. Dickey/
Primary Examiner
Art Unit 2826